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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,716	07/31/2003	Shun-ichi Fukuyama	030860	9374
38834	7590	02/11/2005	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			SMOOT, STEPHEN W	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/630,716

Applicant(s)

FUKUYAMA ET AL.

Examiner

Stephen W. Smoot

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 8-10 is/are rejected.
- 7) ☒ Claim(s) 5-7 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9-2-04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

This Office action is in response to applicant's amendment filed on 15 November 2004.

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 10, line 3, the "second insulating film" as claimed does not particularly point out if this is the same or different from the "second insulating film" as claimed in claim 9, step (c).

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by K. Azuma et al. (JP 2001-274239 A – from applicant's IDS).

Referring to Fig. 4 and paragraphs [0014] to [0034] of the English translation, K. Azuma et al. disclose an interconnect structure with the following features:

- A silicon substrate (1);
- A first insulating film (4) (e.g. silicon dioxide) with a planar top surface formed on the silicon substrate (1);
- A second insulating film (51) (e.g. organic SOG or porous silica) with a low dielectric constant formed on the first insulating film (4);
- A wiring line (8w) formed over the second insulating film (51);

- A metal plug (8p) (e.g. aluminum, copper) formed through the first and second insulating films (4, 51);
- The metal plug (8p) is in contact with a wiring line (8w) as shown in Fig. 4(g) and may also electrically connect the wiring line (8w) to a source/drain diffusion layer of the silicon substrate (1) surface as described in paragraph [0034]; and
- Additional wiring levels are implied by the disclosure of K. Azuma et al. since they show the plug (8p) interconnecting two wiring levels (3, 8w) as shown in Fig. 4(g).

These are all of the limitations set forth in claims 1-4 of the applicant's invention.

Regarding claim 8, the first insulating film (4) may be formed from TEOS or may alternatively be silicon nitride (i.e. protective films) as described in paragraph [0018].

Regarding the method claim 9, the first insulating film (4) may be formed by plasma CVD using TEOS as a source material, the second insulating film (51) can be organic SOG (which implies application by a spin coating process), the plug (8p) is formed by forming an opening (6) through the first and second insulating films (4, 51) as shown in Fig. 8(c) followed by filling the opening (6) with metal as shown in Fig. 8(d), and the wiring line (8w) is formed by forming a gutter (7) in a third insulating film (52) as shown in Fig. 8(e) followed by filling the gutter (7) with metal as shown in Fig. 8(f).

5. Claims 1-4, 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (US 6,838,771 B2).

Referring to Fig. 6 and column 15, line 18 to column 16, line 62, Tanaka et al. disclose a multi-layer wiring structure with the following features:

- A semiconductor substrate (601);
- A BPSG insulating film (605) with a planar top surface formed on the silicon substrate (601);
- A silicon carbonitride film (607) (i.e. a protective film) formed on the BPSG insulating film (605);
- A low dielectric constant spin-on HSQ film (608) (i.e. porous silica) formed on the silicon carbonitride film (607);
- Multiple levels of wiring lines (623) formed over the low dielectric constant spin-on HSQ film (608);
- A metal plug (606) (e.g. copper) formed through the insulating films (605, 607, 608) and interconnecting the lowermost wiring level (623) to the semiconductor substrate (601); and
- As shown in Fig. 6, the insulating films (605, 607, 608) have planar top surfaces.

These are all of the limitations set forth in claims 1-4, 8 of the applicant's invention.

Regarding the method claims 9-10, the BPSG insulating film (605) can be flattened by CMP, the silicon carbonitride film (607) may be formed by CVD, the low dielectric constant spin-on HSQ film (608) is applied by spin-coating, the plug (606) is formed by forming an opening (6) through the insulating films (605, 607, 608) followed

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by filling the opening with copper, and the wiring lines (623) are formed by forming trenches in insulating films followed by filling the trenches with metal.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

***Allowable Subject Matter***

6. Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claims 5-7 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a semiconductor device that includes a conductive connector that is buried in first and second insulating films for interconnecting a wiring pattern to a semiconductor element, with the second insulating film overlying the first insulating film and also having a lower dielectric constant than the first insulating film, wherein a surface modifying layer formed by using silane coupler or metal coupler is formed on an upper surface of the second insulating film and defines a trench bottom corresponding to the wiring pattern.

***Response to Arguments***

8. Applicant's arguments with respect to claims 1-4, 8-10 have been considered but are moot in view of the new grounds of rejection.

***Conclusion***

9. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.



10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWS

*Stephen W. Smoot*  
Patent Examiner  
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